disposed over the floating gates, the control gates of the memory cell in each row being commonly coupled to a word line extending generally parallel to the row[; and], the conductive member being disposed generally parallel to the word line along at least portion of its respective row.

REMARKS

Reconsideration of the above-identified application is requested in view of the remarks that follow:

Applicant has amended the specification of this application, as indicated above, to correct a number of typographical and grammatical errors. No new matter has been added.

In the March 14, 2000, Office Action in this application, the Examiner rejected claim 23 under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor at the time the application was filed had possession of the claimed invention.

As indicated above, claim 23 has been canceled.

The Examiner also rejected claims 1-6, 10-14, 17-18, 20-22, 24 and 26-31 under 35 U.S.C. §103(a) as being unpatentable over the Sung et al. reference. For the reasons set forth below, this rejection is traversed.

With respect to pending claim 1, the Examiner states that the conductive member 40' taught by Sung et al. is "associated with" each of the two rows immediately adjacent because it carries voltage to be applied to the source region shared between these two rows. The Examiner further states with respect to claim 1, that the Sung et al. conductor 40' is associated with two rows and makes contact with the common source region shared between the two rows.

However, the Examiner fails to consider several features of the claimed invention recited in claim 1 and neither taught nor suggested by the Sung et al. reference.

As previously stated in Applicant's remarks to the Patent Office, the present invention relates to a memory array that include memory cells that are arranged in rows and columns and wherein the memory cells in each adjacent row pair have common source regions. In accordance with the invention, a source conductor member is provided for each row pair. Each source conductor member makes contact with the common source region of the respective row pairs. Furthermore, each source conductor is self-aligned with the edges of the bit lines of the adjacent memory cells. This is clearly shown in Fig. 2c of the application, wherein it is shown that the source conductor 112a is self-aligned to the sidewall spacers 144 of the two memory cells shown in Fig 2c. Nothing in the Sung et all reference either teaches or suggests this aspect of the claim 1 invention.

With respect to claim 13, the flash EPROM array recited therein includes a conductive member that is disposed on at least a portion of a first insulating sidewall and makes contact with a contact portion of the substrate that is adjacent to the first insulating sidewall Thus, the conductive member is associated with a first row of memory cells and enables the selective erasing of the memory cells of that row during an erase operation.

The Examiner contends that the Sung et al reference teaches this feature. However, as previously stated, the architecture disclosed by Sung et al. does not provide the capability of selectively erasing one or more rows of memory cells, since it does not teach source conductive members that are connected to the source regions of memory cells of adjacent row pairs and that are independent of each other. Therefore, the Sung et al. reference neither teaches nor suggests the claim 13 invention.

Both of the remaining independent claims now pending in this application, i.e., claim 20 and claim 30, recite either or both of the features discussed above in distinguishing the claim 1 and claim 13 inventions from the Sung et al. reference. That is, claim 20 recites that each of the source

connecting members enables the selective erasing of memory cells of one or both of the corresponding rows during an erase operation. Claim 30 recites that the contact of the conductive member is self-aligned with the memory cells of the portions of the rows. Claim 30 further recites that the conductive member enables the selection of one of the first or second rows during an erase operation. Thus, for the reasons set forth above, it is submitted that both claim 20 and claim 30 also patentably distinguish over the Sung et al. teaching.

The Examiner has also rejected claims 7-9, 15-16, 19, 23 and 32-34 under 35 U.S.C. §103(a) as being unpatentable over the Sung et al. reference, and further in view of the Shrivastava and Juengling references. Since each of claims 7-9, 15-16, 19, 23 and 32-34 depends either directly or indirectly from an independent claim discussed above (i.e claims 1, 13, 20, 30), it is submitted that these claims are also in condition for allowance.

For the reasons set forth above, it is believed that all claims now pending in this application are in compliance with all requirements of 35 U.S.C. §112 and patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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